

A METHOD AND RESULTING STRUCTURE FOR FABRICATING DRAM CELL STRUCTURE USING OXIDE LINE SPACER

ABSTRACT OF THE DISCLOSURE

A method for forming bit line and storage node contacts for a dynamic random access device, e.g., DRAM. Other devices (e.g., Flash, EEPROM) may also be included. The method includes providing a substrate, which has a bit line region and a capacitor contact region. The method also includes forming at least a first gate structure and a second gate structure overlying the substrate. The first gate structure and the second gate structure include an overlying cap. The method also includes forming a conformal dielectric layer overlying the first gate structure, the second gate structure, the bit line region, and the capacitor contact region. The method includes forming an interlayer dielectric material overlying the conformal dielectric layer and planarizing the interlayer dielectric material. The method includes forming a masking layer overlying the planarized interlayer dielectric material and exposing a continuous common region within a portion of the planarized interlayer dielectric material overlying a portion of the first gate structure, a portion of the second gate structure, a portion of the bit line region, and a portion of the capacitor contact region. A first etching process is performed to remove the exposed portion of the planarized interlayer dielectric layer. A second etching process is performed to remove a portion of the conformal dielectric layer on the bit line region and to remove a portion of the conformal dielectric layer on the capacitor contact region while using other portions of the conformal layer as a mask to prevent a portion of the first gate structure and a portion of the second gate structure from being exposed. The method deposits a polysilicon fill material within the continuous common region and overlying the bit line region, the capacitor contact region, the first gate structure, and the second gate structure to cover portions of the bit line region, the capacitor contact region, the first gate structure, and the second gate structure to a predetermined thickness. The method includes planarizing the polysilicon fill material to reduce the predetermined thickness and to simultaneously reduce a thickness of a portion of the interlayer dielectric material